Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended) A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

an inspection area setting unit which divides an area to be inspected into at least two partial inspection areas on the semiconductor wafer, each of which has each of different inspection conditions;

an inspection condition setting unit which sets each inspection ~~conditions~~condition for each partial inspection area that is set by the inspection area setting unit;

an image acquiring system which acquires an image signal from the each partial inspection area on the semiconductor wafer; and

an inspection executing unit which executes an inspection to detect the defect by image-processing the image signal acquired by the image detection acquiring system under the each inspection ~~conditions~~condition which have been set by the inspection condition setting unit, ~~or~~for each partial inspection area set by the inspection area setting unit,

wherein the inspection area setting unit ~~calculates distribution of wiring density in an area to be inspected according to layout data, and~~ divides the area to be inspected into at least the two partial inspection areas~~, with a given partial inspection area having a substantially same calculated wiring density range~~

~~throughout, in order to set partial inspection areas~~areas according to layout data, and the inspection condition setting unit sets the each inspection condition for each partial inspection area so that a false-report rate is a fixed value or less, or a detection rate of a specified defect is a fixed value or more.

Claim 2 (Cancelled)

Claim 3 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected into a cell portion and a non-cell portion according to layout data.

Claim 4 (Original) A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit comprises a display screen for overlaying at least one of a defect distribution map showing distribution of defect positions, a layout pattern, and a detected image of the area to be inspected, on an inspection area setting state, or for displaying at least one of them and the inspection area setting state simultaneously.

Claim 5 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected into a defect output area and a non-output area; and the

inspection executing unit outputs a defect, which exists in the defect output area set by the inspection area setting unit.

Claim 6 (Cancelled)

Claim 7 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit calculates a range of each function block included in an area to be inspected according to the layout data, in order to set the partial inspection areas.

Claims 8 and 9 (Cancelled)

Claim 10 (Currently Amended) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit displays a layout pattern of a whole chip on an inspection area setting screen, and registers an area, which has been specified or has been edited by a user on the layout pattern, as the partial inspection area~~; or~~

~~a user edits the partial inspection area, which has been calculated by the inspection area setting unit, and registers the partial inspection area~~.

Claim 11 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit superimposes each of the partial inspection areas on the layout pattern to display them.

Claim 12 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit superimposes and displays at least two of: each of the partial inspection areas; the layout pattern; and a position where a defect occurred.

Claim 13 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection executing unit classifies detected defects by kind of defect; and

the inspection area setting unit superimposes a position on the layout pattern, where the defect occurred, on the layout pattern by using symbols, which are unique to kinds of defects, to display them.

Claim 14 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection executing unit classifies detected defects according to at least whether the defect is a true defect or a false report.

Claim 15 (Cancelled)

Claim 16 (Currently Amended) A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

an inspection condition setting unit which calculates peculiar inspection ~~conditions~~condition for each position of an area to be inspected on the semiconductor wafer;

an inspection area setting unit which divides the area to be inspected into partial inspection areas on the semiconductor wafer, each of which has the substantially same inspection conditions that are calculated by the inspection condition calculating unit;

an image acquiring system which acquires an image signal from the each partial inspection area on the semiconductor wafer; and

an inspection executing unit which executes an inspection to detect the defect by image-processing the image signal acquired by the image detection acquiring system under the each inspection ~~conditions,~~condition which have been set by the inspection condition setting unit, for each partial inspection area set by the inspection area setting unit,

wherein the inspection area setting unit ~~calculates distribution of wiring density in an area to be inspected according to layout data, and~~ divides the area to be inspected into the partial inspection areas~~, with a given partial inspection area having a substantially same calculated wiring density range throughout, in order to set partial inspection areas~~according to layout data, and the inspection condition setting unit sets the each inspection condition for each partial inspection area so that a false-report rate is a fixed value or less, or detection rate of a specified defect is a fixed value or more.

Claim 17 (Original) A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 16, wherein the inspection area setting unit comprises a display screen for overlaying at least one of a defect distribution map showing distribution of defect positions, a layout pattern, and a

detected image of the area to be inspected, on an inspection area setting state, or for displaying at least one of them and the inspection area setting state simultaneously.

Claim 18 (Original) A system for inspecting a defect of an electronic circuit pattern according to claim 16, wherein the inspection area setting unit divides the area to be inspected into a defect output area and a non-output area; and

the inspection executing unit outputs a defect, which exists in the defect output area set by the inspection area setting unit.

Claim 19 (Cancelled)

Claim 20 (Currently Amended) A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

a pattern inspecting apparatus having a defect extracting unit which ~~determines~~extracts coordinates of a defect position on the semiconductor wafer, and an ~~attribute~~ID of the defect; and

a defect reviewing apparatus having: a partial inspection area data generating unit which generates partial inspection area data according to layout data on the semiconductor wafer,

an inspection ~~area~~condition setting unit which determines an image-detection condition parameter in response to characteristic of a area where the defect position extracted by the defect extracting unit is existed on the semiconductor wafer, based on the partial inspection area data generated by the partial inspection area data

generating unit, ~~divides an area to be inspected into a plurality of partial inspection areas, each of which has a different defect control criterion;~~

~~a defect control criterion setting unit which sets a defect control criterion for each of the partial inspection areas, each of which has a different defect control criterion; and~~

~~a defect classification unit which gives control information to the defect position coordinates, which have been determined by the defect extracting unit, for each defect according to the defect control criterion set by the defect control criterion setting unit, and an attribute of the defect,~~

~~wherein the inspection area setting unit calculates distribution of wiring density in an area to be inspected according to layout data, and divides the area to be inspected into the partial inspection areas, with a given partial inspection area having a substantially same calculated wiring density range throughout, in order to set partial inspection areas~~

an image acquiring system which detects an image signal of the defect under the image-detection condition parameter determined by the inspection condition setting unit, and

a display unit which displays the image signal of the defect acquired by the defect acquiring system, on a screen.

Claim 21 (Currently Amended) A ~~defect inspection control~~ system for inspecting a defect of an electronic circuit pattern according to ~~Claim~~claim 20, wherein ~~the defect extracting unit calculates at least coordinates of a defect position, and a size of a defect;~~

~~the defect control criterion setting unit calculates a critical defect judgment size at each position of the area to be inspected according to layout data; and~~

~~the defect classification unit compares a defect size with the critical defect judgment size, which has been set by the control criterion setting unit, for the defect position coordinates calculated by the defect extracting unit, and gives control information, which indicates whether or not it is critical, to each defect~~in the image detection system, the image-detection condition parameter includes an image-pickup magnification or an image detection mode for specifying whether or not a reference image is detected.

Claim 22 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

a process for reading layout data of an electronic circuit pattern on the semiconductor wafer;

a process for dividing an ~~inspection area of the electronic circuit pattern~~area to be inspected into a plurality of partial inspection areas on the semiconductor wafer according to the read layout data, each of which has each of different inspection conditions;

a process for setting each inspection ~~conditions, which correspond to each inspection area,~~condition for each of the ~~plurality of~~ divided inspection areas;

a process for acquiring an image signal from the each partial inspection area by an image acquiring system;

~~a process for picking up the electronic circuit pattern to acquire an image of the electronic circuit pattern;~~

a process for ~~inspecting each of the inspection areas for the acquired image, using the~~executing an inspection to detect the defect by image-processing the image signal acquired by the image acquiring system under the each inspection ~~conditions~~condition that are set for ~~each of~~ the each partial inspection ~~areas~~area; and

a process for displaying ~~a~~an executed result of the inspection on a screen~~,~~;

wherein ~~the inspection area setting unit calculates distribution of wiring density in an area to be inspected according to layout data, and divides the area to be inspected into the partial inspection areas, with a given partial inspection area having a substantially same calculated wiring density range throughout, in order to set partial inspection areas~~in the process for setting each inspection condition, the each inspection condition for the each partial inspection area is set so that a false-report rate is a fixed value or less, or detection rate of a specified defect is a fixed value or more.

Claim 23 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, the inspection area is divided into the plurality of inspection areas, each of which has different density of the electronic circuit pattern.

Claim 24 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein the layout pattern, which has been divided into the plurality of layout patterns, is displayed on a screen.

Claim 25 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein the layout pattern, which has been divided into the plurality of layout patterns, is identified for each divided area, and is displayed on a screen.

Claim 26 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, a range of each function block included in an area to be inspected is calculated according to the layout data, and thereby the inspection area is divided into the function blocks.

Claim 27 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, distribution of wiring density in an area to be inspected is calculated according to the layout data, and thereby the area to be inspected is divided into areas, each of which has the same calculated wiring density.

Claim 28 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area

into a plurality of inspection areas, an inspection area is divided into areas, each of which has different criticality.

Claim 29 (Original) A method for inspecting a defect of an electronic circuit pattern according to Claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, a layout pattern of a whole chip is displayed on a screen, in addition to it, the layout pattern is divided into areas, each of which has been specified by a user, and then the areas are registered.

Claim 30 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, the inspection area, which has been divided into the plurality of inspection areas, is superimposed on the layout pattern to display them.

Claim 31 (Original) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, from among the inspection area, which has been divided into the plurality of inspection areas, the layout pattern, and a position where a defect occurred, at least two of them are superimposed to display them.

Claim 32 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for ~~inspecting~~

~~each of the inspection areas~~executing the inspection, the detected defects are classified by kind of defect; and

in the process for displaying a~~the executed~~ result of the inspection on a~~the~~ screen, a defect ~~occurrence position~~positions occurred on ~~the~~a layout pattern ~~is~~are superimposed on the layout pattern to display them, using symbols, which are unique to kinds of defects.

Claim 33 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for ~~inspecting each of the inspection areas~~executing the inspection, the detected defects are classified according to at least whether the defect is a true defect or a false report.

Claim 34 (Cancelled)

Claim 35 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern, comprising:

a process for ~~reading position information about a defect of an electronic circuit pattern formed on a substrate, which has been detected by the defect detection unit and stored in a first storage unit~~acquiring coordinate information of a defect position on the semiconductor wafer, and an ID information of the defect, which have been detected by a pattern inspecting apparatus and stored in a first storage unit;

a process for ~~reading layout data of an electronic circuit pattern formed on a substrate from a second storage unit;~~generating partial inspection area data according to layout data on the semiconductor wafer,

a process for ~~creating a layout pattern from the read layout data~~determining a image-detection condition in response to a characteristic of an area where the acquired defect position is existed on the semiconductor wafer, based on the generated partial inspection area data;

a process for acquiring an image signal of the defect under the determined image-detection condition by an image acquiring system, ~~dividing an electronic circuit pattern formed on the substrate into a plurality of areas, using the created layout pattern;~~

~~a process for setting image acquisition conditions for each of the plurality of divided areas;~~

~~a process for picking up the electronic circuit pattern to acquire an image of the defect of the electronic circuit pattern, according to the read position information about the defect of the electronic circuit pattern, and the image acquisition conditions that have been set for each of the plurality of areas;, and~~

a process for displaying ~~an~~the image signal of the ~~acquired~~ defect acquired by the image acquiring system, on a screen,

~~wherein the inspection area setting unit calculates distribution of wiring density in an area to be inspected according to layout data, and divides the area to be inspected into the partial inspection areas, with a given partial inspection area having a substantially same calculated wiring density range throughout, in order to set partial inspection areas.~~

Claim 36 (Cancelled)

Claim 37 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein ~~in~~ the ~~plurality of image acquisition conditions, a condition of image magnification of the electronic circuit pattern, which should be acquired, is included~~image-detection condition includes an image-pickup magnification or an image detection mode for specifying whether or not a reference image is detected.

Claim 38 (Cancelled)

Claim 39 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein ~~in~~ the process for displaying ~~an~~the image signal of ~~a~~the defect ~~on a screen, the image of the defect is classified, and is displayed on the screen~~includes a process for giving classification information to the defect based on the image signal of the defect acquired by the image acquiring system to display the given classification information to the defect on the screen.

Claim 40 (Currently Amended) A method for inspecting a defect of an electronic circuit pattern according to ~~Claim~~claim 35, wherein in the process for ~~dividing an electronic circuit pattern into a plurality of areas, the plurality of areas are divided into a plurality of areas in response to density of the electronic circuit~~

~~pattern~~determining the image-detection condition, the characteristic of a area where the acquired defect position is existed on the semiconductor wafer includes a density of the electronic circuit pattern.

Claims 41 and 42 (Cancelled)

Claim 43 (New) A system for inspecting a defect of an electronic circuit pattern according to claim 20, wherein further comprising a classification unit which gives classification information to the defect based on the image signal of the defect detected by the image detection system to display on the screen of the display unit.

Claim 44 (New) A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection condition setting unit automatically adjusts the each inspection condition for each partial inspection area until the false-report rate is a fixed value or less, or the detection rate of a specified defect is a fixed value or more.

Claim 45 (New) A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 16, wherein the inspection condition setting unit automatically adjusts the each inspection condition for each partial inspection area until the false-report rate is a fixed value or less, or the detection rate of a specified defect is a fixed value or more.

Claim 46 (New) A system for inspecting a defect of an electronic circuit pattern according to claim 20, wherein the inspection condition setting unit automatically adjusts the each inspection condition for each partial inspection area until a false-report rate is a fixed value or less, or a detection rate of a specified defect is a fixed value or more.

Claim 47 (New) A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein the process for setting each inspection condition automatically adjusts the each inspection condition for each partial inspection area until the false-report rate is a fixed value or less, or the detection rate of a specified defect is a fixed value or more.

Claim 48 (New) A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein the process for setting each inspection condition automatically adjusts the each inspection condition for each partial inspection area until a false-report rate is a fixed value or less, or a detection rate of a specified defect is a fixed value or more.